SPECIFICATION FOR LCD MODULE

Model No. _TM0245AKCWF_

Prepared by:	**Date:**
Checked by :	**Date:**
Verified by :	**Date:**
Approved by:	**Date:**

TIANMA MICROELECTRONICS CO., LTD

Ver. 1.1

REVISION RECORD

Date	Ver.	Ref. Page	Revision No.	Revision Items

1. General Specifications:

1.1 Display type: COLOR STN

1.2 Display color*[1]:

Display color: 4K COLOR

Background*[2]: Black (Red, Green, Blue dots are off state)

1.3 Polarizer mode: Transflective/Negative

1.4 Viewing Angle: 6:00

1.5 Driving Method: 1/97 Duty 1/8 Bias

1.6 Backlight Type: LED (2 LAMPS)

Backlight Color: WHITE

1.7 Controller: AR3301-09

1.8 Data Transfer: Parallel

1.9 Operating Temperature: -20～+70℃

Storage Temperature: -30～+80℃

1.10 Power Supply Voltage: VDD=2.65V

1.11 LCD Operating Voltage: VLCD=9.75V

1.12 Outline Dimensions: Refer to outline drawing on next page

1.13 Dot Matrix: 128×3 (RGB)×128 Dots

1.14 Dot Size: 0.215(R+G+B)×0.215(mm^2)

1.15 Dot Pitch: 0.225×0.225 (mm^2)

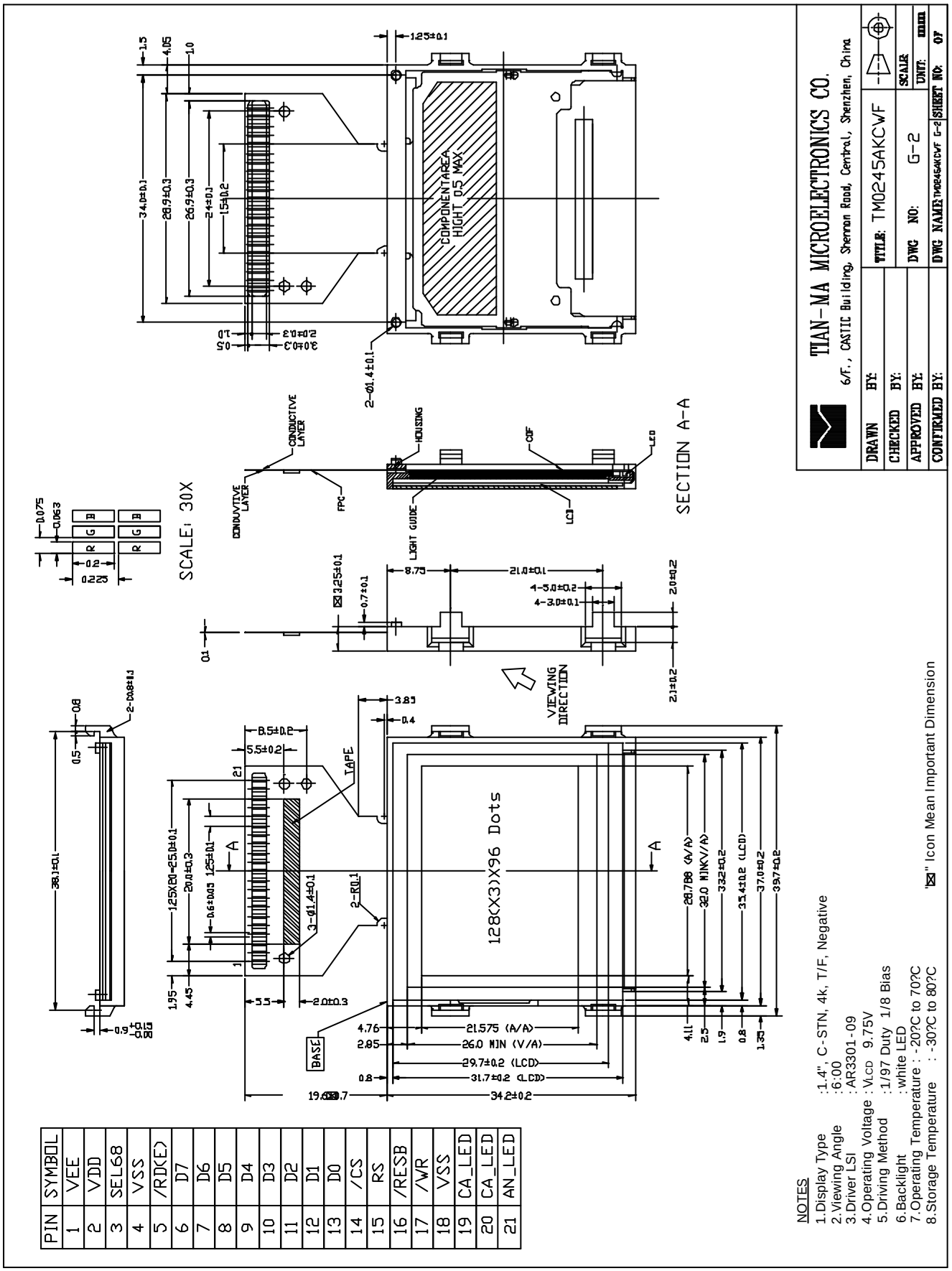
1.16 Weight: TBD*[3]

*[1] Color tone is slightly changed by temperature and driving voltage.

*[2] Color tone will be changed by backlight.

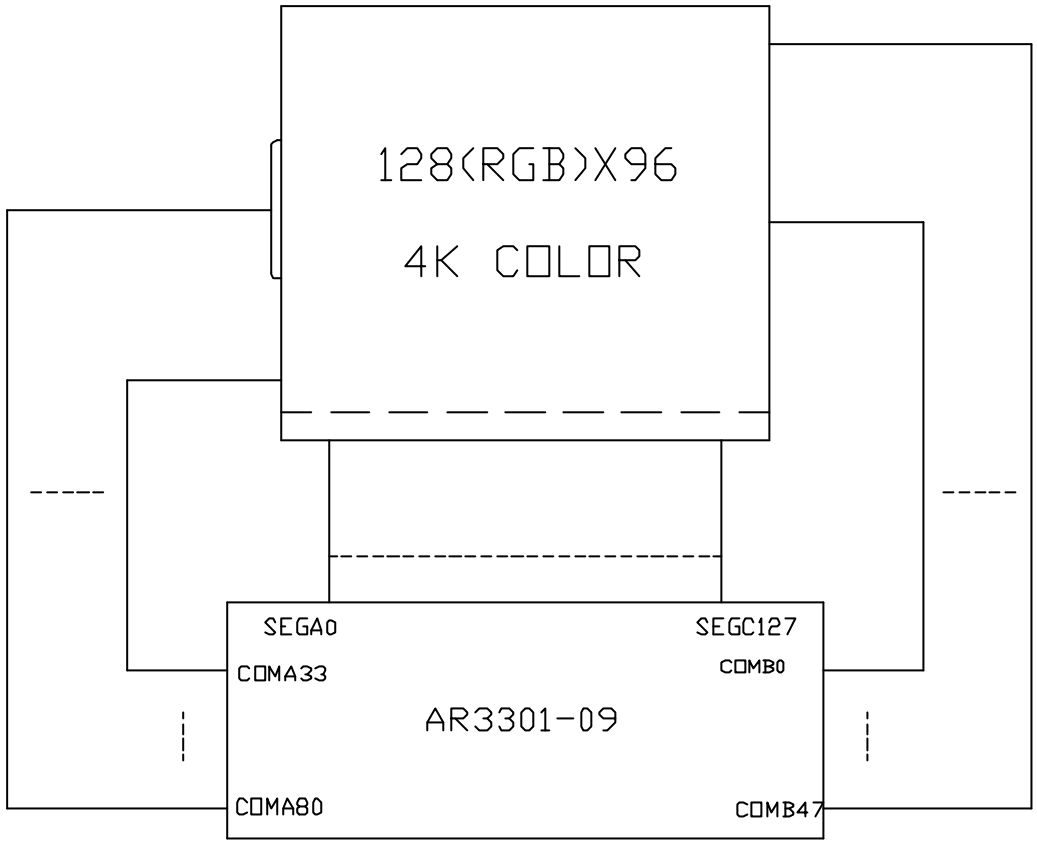
*[3] TBD: To Be Determined.

2. Outline Drawing



PIN	SYMBOL
1	VEE
2	VDD
3	SEL68
4	VSS
5	/RD(E)
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	/CS
15	RS
16	/RESB
17	/WR
18	VSS
19	CA_LED
20	CA_LED
21	AN_LED

NOTES
1. Display Type :1.4", C-STN, 4k, T/F, Negative
2. Viewing Angle :6:00
3. Driver LSI :AR3301-09
4. Operating Voltage : V_{LCD} 9.75V
5. Driving Method :1/97 Duty 1/8 Bias
6. Backlight :white LED
7. Operating Temperature : -20?C to 70?C
8. Storage Temperature : -30?C to 80?C



TIAN-MA MICROELECTRONICS CO. 22/F., HANGDU Building, Shennan Road, Central, Shenzhen, China			
DRAWN BY:		TITLE: TM0245AR	SCALE:
CHECKED BY:		DWG NO: C-1	UNIT: mm
APPROVED BY:		DWG NAME: TM0245AR C-1	SHEET NO: 1 OF 1

3. Absolute Maximum Ratings

Ta=25℃

Item	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	$V_{DD}-V_{SS}$	-0.3	+4.0	V	
LCD Driving Voltage	V_{LCD}	TBD	+20.0		
Operating Temperature Range	T_{OP}	-20	+70	℃	No Condensation
Storage Temperature Range	T_{ST}	-30	+80		

4. Electrical Specifications and Instruction Code

4.1 Electrical characteristics Vss=0V, Ta=25℃

Item		Symbol	Min.	Typ.	Max.	Unit
Supply Voltage (Logic)		V_{DD}-Vss	2.8	3	3.3	V
Supply Voltage		V_{EE}	-	2.65	-	V
Supply Voltage (LCD Drive)		V_{LCD}	-	9.75	-	V
Input Signal Voltage	High	V_{IH} (V_{DD}=3.0)	0.8V_{DD}	-	V_{DD}	V
	Low	V_{IL} (V_{DD}=3.0)	0	-	0.2 V_{DD}	V
Supply current (Logic)		I_{DD} (V_{DD}- V_{SS}=3.0V)	-	TBD	-	mA
Operating current		I_{op}	-	TBD	-	mA
Supply Voltage (LED)		V_{LED}	-	5	-	V
Supply current (LED)		I_{LED}	-	30.0	40	mA

4.2 Interface Pin Funtion

Pin No.	Symbol	Description
1	VEE	VEE level pin for LCD boost driving
2	VDD	VDD level pin for logic driving
3	SEL68	CPU inter face selection port
4	Vss	Ground level pin
5	/RD(E)	Read control input pin
6	D7	Data bus
7	D6	
8	D5	
9	D4	
10	D3	
11	D2	
12	D1	
13	D0	
14	/CS	Chip select input pin for main LCD
15	RS	Register select pin
16	/RESB	Reset signal input pin
17	/WR	Write control input pin
18	VSS	Ground level pin
19	CA_LED	LED back light for main LCD(Cathode)
20	CA_LED	LED back light for main LCD(Cathode)
21	AN_LED	All LED back light(Anode)

4.3 Interface Timing Chart

Data Write to Display RAM and Control Register

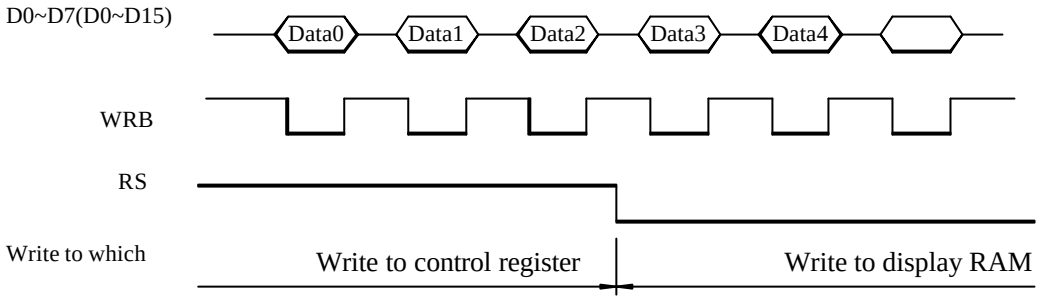
The data write to display RAM and Control Register use almost same procedure.. It is determined by the state of RS.

RS="L": display RAM data

RS="H": control register data

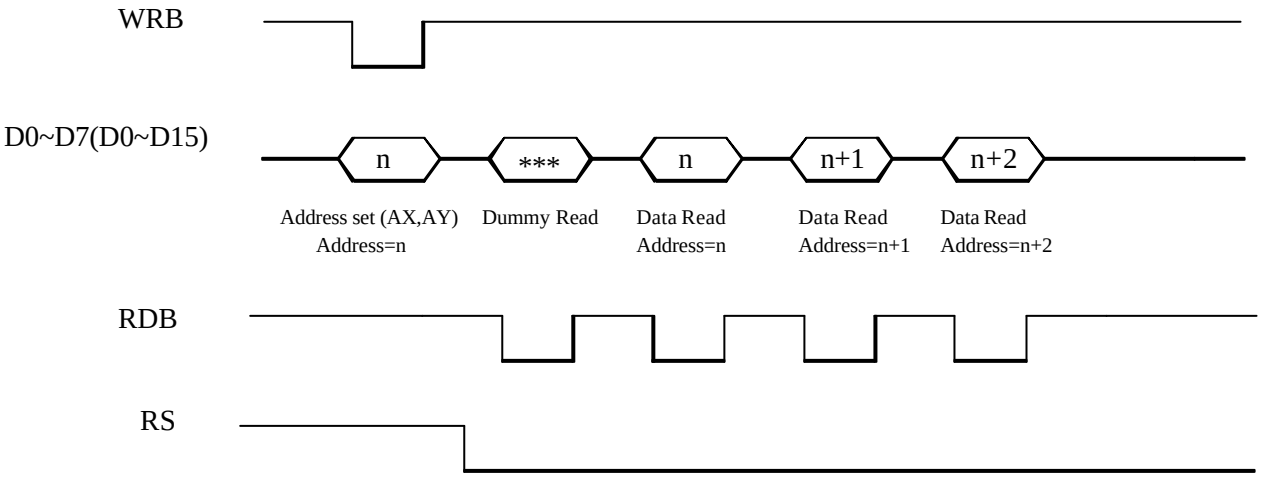
Incaseof the 80-damily MPU, the data is written at the rising edge of WRB. In case of the 68-family MPU, the data is written at the falling edge of signal E.

Data write operation



Internal Register Read

In case of display RAM read operation ,need dummy read one time. The designated address data are not output to the read operation immediately after the address set to AX or AY register, but Dummy read is always required one time after address set and writer cycle.



4.4 Instruction code

Control Register Table (Bank 0)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
X Address (Lower nibble) [0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper nibble) [1H]	0	1	0	1	0	0	0	0	0	0	1	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
Y Address (Lower nibble) [2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of Y direction Address in display RAM
Y Address (Upper nibble) [3H]	0	1	0	1	0	0	0	0	0	1	1	AY7	AY6	AY5	AY4	Set of Y direction Address in display RAM
Display start address (Lower nibble) [4H]	0	1	0	1	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Set address of display RAM making common starting line display
Display start address (Upper nibble) [5H]	0	1	0	1	0	0	0	0	1	0	1	LA7	LA6	LA5	LA4	Set address of display RAM making common starting line display
n-line alternation (Lower nibble) [6H]	0	1	0	1	0	0	0	0	1	1	0	N3	N2	N1	N0	Set the number of alternated reverse line
n-line alternation (Upper nibble) [7H]	0	1	0	1	0	0	0	0	1	1	1	N7	N6	N5	N4	Set the number of alternated reverse line
Display control (1) [8H]	0	1	0	1	0	0	0	1	0	0	0	SHIFT0	MON	ALLON	ON/OFF	SHIFT0: Select order direction. MON: Select Monochrome/gradation ALLON: All display ON ON/OFF: Display ON/OFF control
Display control (2) [9H]	0	1	0	1	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Display normal/reverse NLIN: n line reverse control SWAP: Display data swapping REF: Segment normal/reverse
Increment control [AH]	0	1	0	1	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Select window, AIM: Select increment mode AYI:Y increment, AXI:X increment
Power control [BH]	0	1	0	1	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Internal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio [CH]	0	1	0	1	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Set LCD drive duty ratio
Booster [DH]	0	1	0	1	0	0	0	1	1	0	1	※	VU2	VU1	VU0	Set number of boosting step for booster circuit
Bias ratio control [EH]	0	1	0	1	0	0	0	1	1	1	0	※	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LSI test, must set to "0" RE: set register bank number

Note: The "※" mark means "don't care".
Parentheses [ ] shows address for control register.

Control Register Table (Bank 1)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette A0/A8 (Lower nibble) [0H]	0	1	0	1	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Set the number of Gradation Palette A0(PS=0)/A8(PS=1)
Gradation palette A0/A8 (Upper nibble) [1H]	0	1	0	1	0	0	1	0	0	0	1	※	※	※	PA04/ PA84	Set the number of Gradation Palette A0(PS=0)/A8(PS=1)
Gradation palette A1/A9 (Lower nibble) [2H]	0	1	0	1	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Set the number of Gradation Palette A1(PS=0)/A9(PS=1)
Gradation palette A1/A9 (Upper nibble) [3H]	0	1	0	1	0	0	1	0	0	1	1	※	※	※	PA14/ PA94	Set the number of Gradation Palette A1(PS=0)/A9(PS=1)
Gradation palette A2/A10 (Lower nibble) [4H]	0	1	0	1	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Set the number of Gradation Palette A2(PS=0)/A10(PS=1)
Gradation palette A2/A10 (Upper nibble) [5H]	0	1	0	1	0	0	1	0	1	0	1	※	※	※	PA24/ PA104	Set the number of Gradation Palette A2(PS=0)/A10(PS=1)
Gradation palette A3/A11 (Lower nibble) [6H]	0	1	0	1	0	0	1	0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110	Set the number of Gradation Palette A3(PS=0)/A11(PS=1)
Gradation palette A3/A11 (Upper nibble) [7H]	0	1	0	1	0	0	1	0	1	1	1	※	※	※	PA24/ PA114	Set the number of Gradation Palette A3(PS=0)/A11(PS=1)
Gradation palette A4/A12 (Lower nibble) [8H]	0	1	0	1	0	0	1	1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120	Set the number of Gradation Palette A4(PS=0)/A12(PS=1)
Gradation palette A4/A12 (Upper nibble) [9H]	0	1	0	1	0	0	1	1	0	0	1	※	※	※	PA44/ PA124	Set the number of Gradation Palette A4(PS=0)/A12(PS=1)
Gradation palette A5/A13 (Lower nibble) [AH]	0	1	0	1	0	0	1	1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130	Set the number of Gradation Palette A5(PS=0)/A13(PS=1)
Gradation palette A5/A13 (Upper nibble) [BH]	0	1	0	1	0	0	1	1	0	1	1	※	※	※	PA54/ PA134	Set the number of Gradation Palette A5(PS=0)/A13(PS=1)
Gradation palette A6/A14 (Lower nibble) [CH]	0	1	0	1	0	0	1	1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140	Set the number of Gradation Palette A6(PS=0)/A14(PS=1)
Gradation palette A6/A14 (Upper nibble) [DH]	0	1	0	1	0	0	1	1	1	0	1	※	※	※	PA64/ PA144	Set the number of Gradation Palette A6(PS=0)/A14(PS=1)
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LSI test, must set to "0" RE: set register bank number

Note: The "※" mark means "don't care".
Parentheses [ ] shows address for control register.

Control Register Table (Bank 2)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette A7/A15 (Lower nibble) [0H]	0	1	0	1	0	1	0	0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150	Set the number of Gradation Palette A7(PS=0)/A15(PS=1)
Gradation palette A7/A15 (Upper nibble) [1H]	0	1	0	1	0	1	0	0	0	0	1	※	※	※	PA74/ PA154	Set the number of Gradation Palette A7(PS=0)/A15(PS=1)
Gradation palette B0/B8 (Lower nibble) [2H]	0	1	0	1	0	1	0	0	0	1	0	PB03/ PB83	PB02 / PB82	PB01 / PB81	PB00/ PB80	Set the number of Gradation Palette B0(PS=0)/B8(PS=1)
Gradation palette B0/B8 (Upper nibble) [3H]	0	1	0	1	0	1	0	0	0	1	1	※	※	※	PB04/ PB84	Set the number of Gradation Palette B0(PS=0)/B8(PS=1)
Gradation palette B1/B9 (Lower nibble) [4H]	0	1	0	1	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Set the number of Gradation Palette B1(PS=0)/B9(PS=1)
Gradation palette B1/B9 (Upper nibble) [5H]	0	1	0	1	0	1	0	0	1	0	1	※	※	※	PB14/ PB94	Set the number of Gradation Palette B1(PS=0)/B9(PS=1)
Gradation palette B2/B10 (Lower nibble) [6H]	0	1	0	1	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB10 2	PB21 / PB10 1	PB20/ PB100	Set the number of Gradation Palette B2(PS=0)/B10(PS=1)
Gradation palette B2/B10 (Upper nibble) [7H]	0	1	0	1	0	1	0	0	1	1	1	※	※	※	PB24/ PB104	Set the number of Gradation Palette B2(PS=0)/B10(PS=1)
Gradation palette B3/B11 (Lower nibble) [8H]	0	1	0	1	0	1	0	1	0	0	0	PB33/ PB113	PB32 / PB112	PB31 / PB111	PB30/ PB110	Set the number of Gradation Palette B3(PS=0)/B11(PS=1)
Gradation palette B3/B11 (Upper nibble) [9H]	0	1	0	1	0	1	0	1	0	0	1	※	※	※	PB24/ PB114	Set the number of Gradation Palette B3(PS=0)/B11(PS=1)
Gradation palette B4/B12 (Lower nibble) [AH]	0	1	0	1	0	1	0	1	0	1	0	PB43/ PB123	PB42 / PB12 2	PB41 / PB12 1	PB40/ PB120	Set the number of Gradation Palette B4(PS=0)/B12(PS=1)
Gradation palette B4/B12 (Upper nibble) [BH]	0	1	0	1	0	1	0	1	0	1	1	※	※	※	PB44/ PB124	Set the number of Gradation Palette B4(PS=0)/B12(PS=1)
Gradation palette B5/B13 (Lower nibble) [CH]	0	1	0	1	0	1	0	1	1	0	0	PB53/ PB133	PB52 / PB13 2	PB51 / PB13 1	PB50/ PB130	Set the number of Gradation Palette B5(PS=0)/B13(PS=1)
Gradation palette B5/B13 (Upper nibble) [DH]	0	1	0	1	0	1	0	1	1	0	1	※	※	※	PB54/ PB134	Set the number of Gradation Palette B5(PS=0)/B13(PS=1)
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LSI test, must set to "0" RE: set register bank number

Note: The "※" mark means "don't care".
Parentheses [ ] shows address for control register.

Control Register Table (Bank 3)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette B6/B14 (Lower nibble) [0H]	0	1	0	1	0	1	1	0	0	0	0	PB63/ PB143	PB62 / PB142	PB61 / PB141	PB60/ PB140	Set the number of Gradation Palette B6(PS=0)/B14(PS=1)
Gradation palette B6/B14 (Upper nibble) [1H]	0	1	0	1	0	1	1	0	0	0	1	※	※	※	PB64/ PB144	Set the number of Gradation Palette B6(PS=0)/B14(PS=1)
Gradation palette B7/B15 (Lower nibble) [2H]	0	1	0	1	0	1	1	0	0	1	0	PB73/ PB153	PB72 / PB152	PB71 / PB151	PB70/ PB150	Set the number of Gradation Palette B7(PS=0)/B15(PS=1)
Gradation palette B7/B15 (Upper nibble) [3H]	0	1	0	1	0	1	1	0	0	1	1	※	※	※	PB74/ PB154	Set the number of Gradation Palette B7(PS=0)/B15(PS=1)
Gradation palette C0/C8 (Lower nibble) [4H]	0	1	0	1	0	1	1	0	1	0	0	PC03 / PC83	PC02 / PC82	PC01 / PC81	PC00 / PC80	Set the number of Gradation Palette C0(PS=0)/C8(PS=1)
Gradation palette C0/C8 (Upper nibble) [5H]	0	1	0	1	0	1	1	0	1	0	1	※	※	※	PC04 / PC84	Set the number of Gradation Palette C0(PS=0)/C8(PS=1)
Gradation palette C1/C9 (Lower nibble) [6H]	0	1	0	1	0	1	1	0	1	1	0	PC13 / PC93	PC12/ PC92	PC11/ PC91	PC10 / PC90	Set the number of Gradation Palette C1(PS=0)/C9(PS=1)
Gradation palette C1/C9 (Upper nibble) [7H]	0	1	0	1	0	1	1	0	1	1	1	※	※	※	PC14 / PC94	Set the number of Gradation Palette C1(PS=0)/C9(PS=1)
Gradation palette C2/C10 (Lower nibble) [8H]	0	1	0	1	0	1	1	1	0	0	0	PC23 / PC103	PC22/ PC102	PC21 / PC101	PC20 / PC100	Set the number of Gradation Palette C2(PS=0)/C10(PS=1)
Gradation palette C2/C10 (Upper nibble) [9H]	0	1	0	1	0	1	1	1	0	0	1	※	※	※	PC24 / PC104	Set the number of Gradation Palette C2(PS=0)/C10(PS=1)
Gradation palette C3/C11 (Lower nibble) [AH]	0	1	0	1	0	1	1	1	0	1	0	PC33 / PC113	PC32 / PC112	PC31 / PC111	PC30 / PC110	Set the number of Gradation Palette C3(PS=0)/C11(PS=1)
Gradation palette C3/C11 (Upper nibble) [BH]	0	1	0	1	0	1	1	1	0	1	1	※	※	※	PC24 / PC114	Set the number of Gradation Palette C3(PS=0)/C11(PS=1)
Gradation palette C4/C12 (Lower nibble) [CH]	0	1	0	1	0	1	1	1	1	0	0	PC43 / PC123	PC42 / PC122	PC41 / PC121	PC40 / PC120	Set the number of Gradation Palette C4(PS=0)/C12(PS=1)
Gradation palette C4/C12 (Upper nibble) [DH]	0	1	0	1	0	1	1	1	1	0	1	※	※	※	PC44 / PC124	Set the number of Gradation Palette C4(PS=0)/C12(PS=1)
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LSI test, must set to "0" RE: set register bank number

Note: The "※" mark means "don't care".
Parentheses [ ] shows address for control register.

Control Register Table (Bank 4)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette C5/C13 (Lower nibble) [0H]	0	1	0	1	1	0	0	0	0	0	0	PC53 / PC133	PC52 / PC132	PC51 / PC131	PC50 / PC130	Set the number of Gradation Palette C5(PS=0)/C13(PS=1)
Gradation palette C5/C13 (Upper nibble) [1H]	0	1	0	1	1	0	0	0	0	0	1	※	※	※	PC54 / PC134	Set the number of Gradation Palette C5(PS=0)/C13(PS=1)
Gradation palette C6/C14 (Lower nibble) [2H]	0	1	0	1	1	0	0	0	0	1	0	PC63 / PC143	PC62 / PC142	PC61 / PC141	PC60 / PC140	Set the number of Gradation Palette C6(PS=0)/C14(PS=1)
Gradation palette C6/C14 (Upper nibble) [3H]	0	1	0	1	1	0	0	0	0	1	1	※	※	※	PC64 / PC144	Set the number of Gradation Palette C6(PS=0)/C14(PS=1)
Gradation palette C7/C15 (Lower nibble) [4H]	0	1	0	1	1	0	0	0	1	0	0	PC73 / PC153	PC72 / PC152	PC71 / PC151	PC70 / PC150	Set the number of Gradation Palette C7(PS=0)/C15(PS=1)
Gradation palette C7/C15 (Upper nibble) [5H]	0	1	0	1	1	0	0	0	1	0	1	※	※	※	PC74 / PC154	Set the number of Gradation Palette C7(PS=0)/C15(PS=1)
Display start common [6H]	0	1	0	1	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Set Common Driver Start Line
Display control [7H]	0	1	0	1	1	0	0	0	1	1	1	IL	DVSE	DSE	SON	IL:Interlace scanning SON:Output control (LP,FLM,M,CLK) DSE:duty select 0:even,1:odd DVSE:divider ratio (1/96,97duty)
Display Select Control [8H]	0	1	0	1	1	0	0	1	0	0	0	PWM	C256	FDC 1	FDC 0	PWM : gradation mode select C256 : 256 color, FDC : booster clock control
RAM Data length Set [9H]	0	1	0	1	1	0	0	1	0	0	1	HSW	ABS	CKS	WLS	HSW : RAM access ABS : selection of 12bit data CKS:osclation circuit WLS:Set data length on RAM access
Electronic Volume (Lower nibble) [AH]	0	1	0	1	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Set Electronic Volume Register (lower code)
Electronic Volume (Upper nibble) [BH]	0	1	0	1	1	0	0	1	0	1	1	※	DV6	DV5	DV4	Set Electronic Volume Register (upper code)
Register read address [CH]	0	1	0	1	1	0	0	1	1	0	0	RA3	RA2	RA1	RA0	Set Register Address for read
Select Rf [DH]	0	1	0	1	1	0	0	1	1	0	1	※	RF2	RF1	RF0	Select Rf ratio of OSC circuit
Discharge control [EH]	0	1	0	1	1	0	0	1	1	1	0	※	※	DIS 2	DIS	DIS:Discharge capacitance of V0,V1,V2,V3,V4 Pins DIS2:Discharge capacitance of VOUT Pins
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LSI test, must set to "0" RE: set register bank number

Note: The "※" mark means "don't care".
Parentheses [ ] shows address for control register.

Control Register Table (Bank 5)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Window X End Address (Lower nibble) [0H]	0	1	0	1	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Set X end address for window function access
Window X End Address (Upper nibble) [1H]	0	1	0	1	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Set X end address for window function access
Window Y End Address (Lower nibble) [2H]	0	1	0	1	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Set Y end address for window function access
Window Y End Address (Upper nibble) [3H]	0	1	0	1	1	0	1	0	0	1	1	EY7	EY6	EY5	EY4	Set Y end address for window function access
Start Address for line reverse (Lower nibble) [4H]	0	1	0	1	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Set start line for line reverse display
Start Address for line reverse (Upper nibble) [5H]	0	1	0	1	1	0	1	0	1	0	1	LS7	LS6	LS5	LS4	Set start line for line reverse display
End Address for line reverse (Lower nibble) [6H]	0	1	0	1	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Set end line for line reverse display
End Address for line reverse (Upper nibble) [7H]	0	1	0	1	1	0	1	0	1	1	1	LE7	LE6	LE5	LE4	Set end line for line reverse display
Line reverse control [8H]	0	1	0	1	1	0	1	1	0	0	0	※	※	BT	LREV	BT: Reverse type select LREV: Line reverse control
Select Address for special Segment [9H]	0	1	0	1	1	0	1	1	0	0	1	※	※	DMY	PS	DMY: Select address for special segment driver. PS :Pallet select upper/lower
PWM mode control [AH]	0	1	0	1	1	0	1	1	0	1	0	PWM G1	PWM G0	PWM R1	PWM R0	PWM mode select
PWM mode control [BH]	0	1	0	1	1	0	1	1	0	1	1	SHI FT2	SHI FT1	PWM B1	PWM B0	PWM mode select
Bias level V1control [CH]	0	1	0	1	1	0	1	1	1	0	0	VS W1	BV 12	BV 11	BV 10	V1 level adjustment
Bias level V4 control [DH]	0	1	0	1	1	0	1	1	1	0	1	VS W4	BV 42	BV 41	BV 40	V4 level adjustment
V1,V4 bias control [EH]	0	1	0	1	1	0	1	1	1	1	0	BST	BPS	BP	BUP	Bias V1,V4 control
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LSI test, must set to "0" RE: set register bank number

Note: The "※" mark means "don't care".
Parentheses [ ] shows address for control register.

Control Register Table (Bank 6)

Control Register	Pins(for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
RGB arrangement [1H]	0	1	0	1	1	0	1	0	0	0	1	S2	S1	S0	asi	Set RGB arrangement

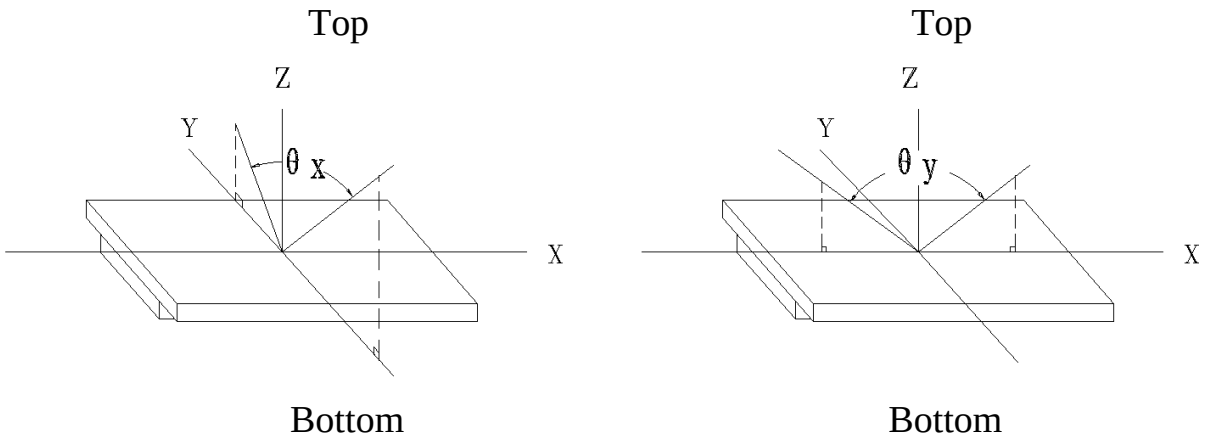
5. Optical Characteristics

5.1 Optical Characteristics V_{LCD}=9.75V Ta=25℃

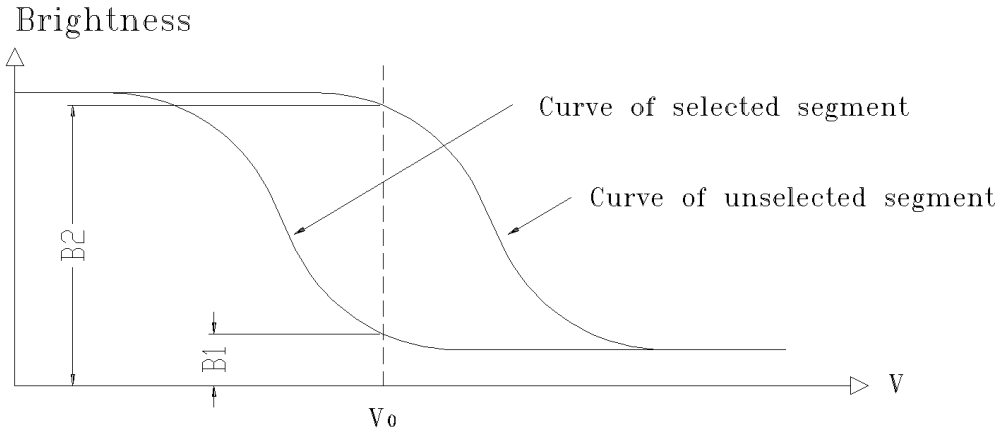
Item		Symbol	Condition		Min.	Typ.	Max.	Unit
Viewing Angle		q_x	Cr=2	$q_y = 0^o$	-30~+45			Deg
		q_y		$q_x = 0^o$	-45~+45			
Contrast Ratio		Cr	$q_x = 0^o$ $q_y = 0^o$		15	-	-	
Response Time	Turn on	Ton	$q_x = 0^o$ $q_y = 0^o$		-	-	200	ms
	Turn off	Toff			-	-	100	
Color Of CIE Coord-inate	Red	x	$q_x = 0^o$ $q_y = 0^o$		-	0.368	-	±0.04
		y			-	0.291	-	
	Green	x	$q_x = 0^o$ $q_y = 0^o$		-	0.286	-	
		y			-	0.383	-	
	Blue	x	$q_x = 0^o$ $q_y = 0^o$		-	0.184	-	
		y			-	0.190	-	
	White	x	$q_x = 0^o$ $q_y = 0^o$		-	0.281	-	
		y			-	0.304	-	

5.2 Definition of Optical Characteristics

5.2.1 Definition of Viewing Angle



5.2.2 Definition of Contrast Ratio

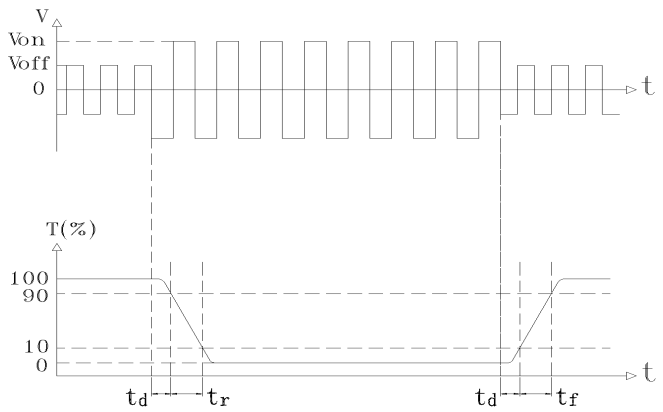


$$\text{Contrast Ratio} = B2/B1 = \frac{\text{unselected state brightness}}{\text{selected state brightness}} \quad 1$$

Measuring Conditions:

1) Ambient Temperature: 25℃ ; 2) Frame frequency: 70Hz

5.2.3 Definition of Response time



Turn on time: $t_{on} = t_d + t_r$ Turn off time: $t_{off} = t_d + t_f$

Measuring Condition:

1) Operating Voltage:9.75V 2) Frame frequency: 70Hz

5.3 Brightness Characteristic

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Brightness	Bp	Ta=25℃±3℃ 30-80%RH	80	-	-	cd/m^2
Uniformity	△Bp		70	-	-	%

Note:

1. The data is measured after LEDs are turned on for 5 minutes.
2. Testing conditions LED : V_{LED}=3.5 V (DC)
   LCD: All dots are on (White color)
3. Brightness in the center of the LCD panel.
4. Definition of Uniformity (△Bp)
   △Bp = Bp (Min.) / Bp (Max.)✕100 (%)
   Bp (Max.) = Maximum brightness in 9 measurement spots
   Bp (Min.) = Minimum brightness in 9 measurement spots

6. Reliability

6.1 Content of Reliability Test Ta=25℃

No.	Test Item	Content of Test	Test condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	80℃±2℃ 240H Restore 4H at 25℃
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-30℃±2℃ 240H Restore 4H at 25℃
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	70℃±2℃ 240H Restore 4H at 25℃
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	-20℃±2℃ 240H Restore 4H at 25℃
5	High Temperature /Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time	70℃±2℃ 90%RH 240H Restore 4H at 25℃
6	Temperature Cycle	Endurance test applying the low and high temperature cycle -30℃←→25℃←→80℃←→25℃ 30min 5min 30min 5min ←——————→ 1 cycle	-30℃/80℃ 10 cycles Restore 4H at 25℃
7	Vibration Test (package state)	Endurance test applying the vibration during transportation	10Hz~150Hz, 100m/s^2, 120min
8	Shock Test (package state)	Endurance test applying the shock during transportation	Half- sine wave, 300m/s^2, 18ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	25kPa 16H Restore 2H

6.2 Failure Judgment Criterion

Criterion Item	Test Item No.									Failure Judgement Criterion
	1	2	3	4	5	6	7	8	9	
Basic Specification	v	v	v	v	v	v	v	v	v	Out of the basic Specification
Electrical specification	v	v	v	v	v					Out of the electrical specification
Mechanical Specification							v	v		Out of the mechanical specification
Optical Characteristic	v	v	v	v	v	v			v	Out of the optical specification
Note	For test item refer to7.1									
Remark	Basic specification = Optical specification + Mechanical specification									

7. Quality Level

Examination or Test	At T_a=25℃ (unless otherwise stated)	Inspection				
		Min.	Max.	Unit	IL	AQL
External Visual Inspection	Under normal illumination and eyesight condition, the distance between eyes and LCD is 25cm.	See Appendix A			II	Major 1.0 Minor 2.5
Display Defects	Under normal illumination and eyesight condition, display on inspection.	See Appendix B			II	Major 1.0 Minor 2.5
Note: Major defects: Open segment or common, Short, Serious damages, Leakage Miner defects: Others Sampling standard conforms to GB2828						

8. Precautions for Use of LCD Modules

8.1 Handling Precautions

8.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

8.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

8.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

8.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

8.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

8.1.6 Do not attempt to disassemble the LCD Module.

8.1.7 If the logic circuit power is off, do not apply the input signals.

8.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

8.2 Storage precautions

8.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

8.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

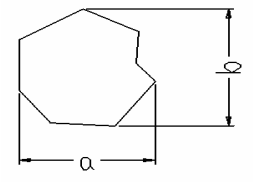
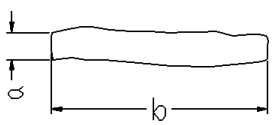
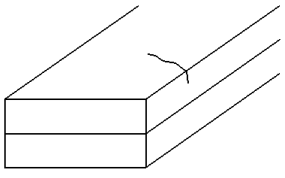
Relatively humidity: ≤80%

8.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

8.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

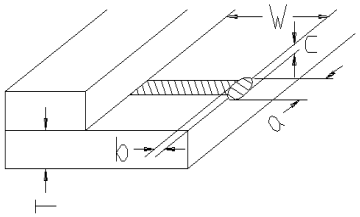
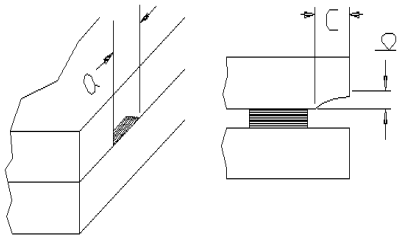
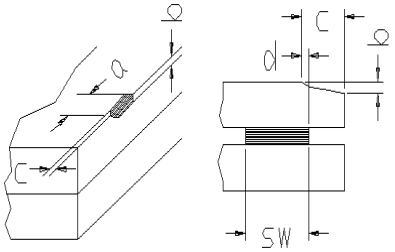
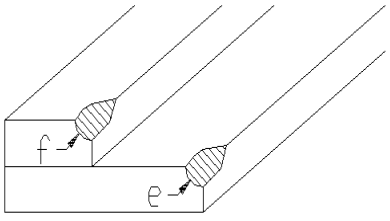
Appendix A

Inspection items and criteria for appearance defects

<table>
<tr><td>Items</td><td>Contents</td><td colspan="4">Criteria</td></tr>
<tr><td>Leakage</td><td></td><td colspan="4">Not permitted</td></tr>
<tr><td>Rainbow</td><td></td><td colspan="4">According to the limit specimen</td></tr>
<tr><td rowspan="4">Polarizer</td><td>Wrong polarizer attachment</td><td colspan="4">Not permitted</td></tr>
<tr><td rowspan="2">Bubble between polarizer and glass</td><td colspan="2">Not counted</td><td colspan="2">Max. 3 defects allowed</td></tr>
<tr><td colspan="2">ϕ<0.3mm</td><td colspan="2">0.3mm≤ϕ≤0.5mm</td></tr>
<tr><td>Scratches of polarizer</td><td colspan="4">According to the limit specimen</td></tr>
<tr><td rowspan="3">Black spot (in viewing area)</td><td rowspan="3"> 
</td><td>Not counted</td><td>Max. 3 spots allowed</td><td rowspan="4">Max. 3 spots (lines) allowed</td></tr>
<tr><td>X<0.2mm</td><td>0.2mm≤X≤0.5mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">Black line (in viewing area)</td><td rowspan="2"> 
</td><td>Not counted</td><td>Max. 3 lines allowed</td></tr>
<tr><td>a<0.02mm</td><td>0.02mm≤a≤0.05mm
b≤2.0mm</td></tr>
<tr><td>Progressive cracks</td><td>  </td><td colspan="4">Not permitted</td></tr>
</table>

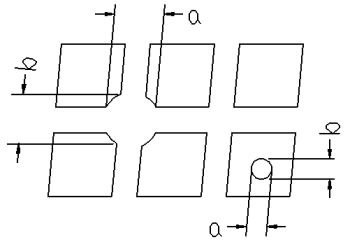
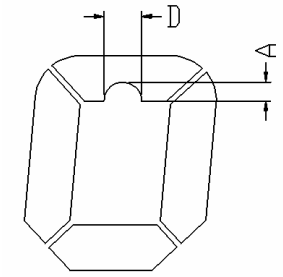
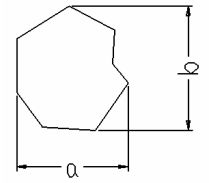
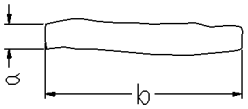
Appendix A

Inspection item and criteria for appearance defects (continued)

<table>
<tr><th>Items</th><th>Contents</th><th colspan="4">Criteria</th></tr>
<tr><td rowspan="4">Glass Cracks</td><td>Cracks on pads
 
</td><td>a
≤3mm
≤2mm</td><td>b
≤W/5
≤W/5</td><td>c
≤T/2
T/2<C<T</td><td>Max. 2 cracks allowed</td><td rowspan="4">Max. 5 cracks allowed</td></tr>
<tr><td>Cracks on contact side
 
</td><td colspan="2">a
≤3mm
≤2mm
C shall be not reach the seal area</td><td>b
≤T/2
T/2<b<T</td><td rowspan="2">Max. 2 cracks allowed</td></tr>
<tr><td>Cracks on non-contact side
 
</td><td colspan="2">a
≤3mm
≤2mm
C≤0.5mm
d≤SW/3</td><td>b
≤T/2
T/2<b<T</td></tr>
<tr><td>Corner cracks
 
</td><td colspan="2">e<2.0mm^2
f<2.0mm^2</td><td>Max. 3 cracks allowed</td></tr>
</table>

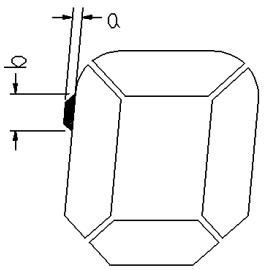
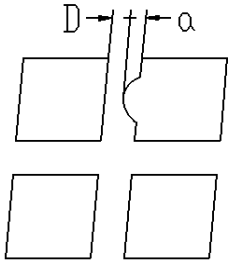
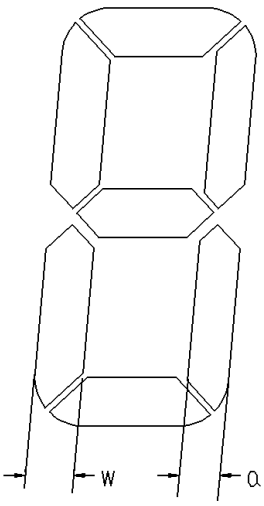
Appendix B

Inspection items and criteria for display defects

<table>
<tr><td colspan="2">Items</td><td>Contents</td><td colspan="3">Criteria</td></tr>
<tr><td colspan="3">Open segment or open common</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Short</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Wrong viewing angle</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Contrast radio uneven</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td colspan="3">Crosstalk</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="4">Pin holes and cracks in segment (DOT)</td><td rowspan="2">  </td><td>Not counted</td><td>Max.3 dots allowed</td><td rowspan="4">Max.3 dots allowed</td></tr>
<tr><td>X<0.1mm</td><td>0.1mm≤X≤0.2mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">  </td><td>Not counted</td><td>Max.2 dots allowed</td></tr>
<tr><td>A<0.1mm</td><td>0.1mm≤A≤0.2mm
D<0.25mm</td></tr>
<tr><td rowspan="3">Black spot (in viewing area)</td><td rowspan="3">  </td><td>Not counted</td><td>Max.3 spots allowed</td><td rowspan="4">Max.3 spots (lines) allowed</td></tr>
<tr><td>X<0.1mm</td><td>0.1mm≤X≤0.2mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">Black line (in viewing area)</td><td rowspan="2">  </td><td>Not counted</td><td>Max.3 lines allowed</td></tr>
<tr><td>a<0.02mm</td><td>0.02mm≤a≤0.05mm
b≤0.5mm</td></tr>
</table>

Appendix B

Inspection items and criteria for display defects (continued)

<table>
<tr><td>Items</td><td>Content</td><td colspan="3">Criteria</td></tr>
<tr><td rowspan="3">Transfor-
mation
of segment</td><td rowspan="2">  </td><td>Not counted</td><td>Max. 2 defects allowed</td><td rowspan="2">Max.3
defects
allowed</td></tr>
<tr><td>x＜0.1mm</td><td>0.1mm≦x≦0.2mm</td></tr>
<tr><td colspan="2">x=(a+b)/2</td></tr>
<tr><td>  </td><td>Not counted</td><td>Max. 1 defects allowed</td><td rowspan="2">Max.3
defects
allowed</td></tr>
<tr><td>a＜0.1mm</td><td>0.1mm≦a≦0.2mm
D>0</td></tr>
<tr><td>  </td><td colspan="3">Max.2 defects allowed
0.8W≦a≦1.2W

a=measured value of width
W=nominal value of width</td></tr>
</table>